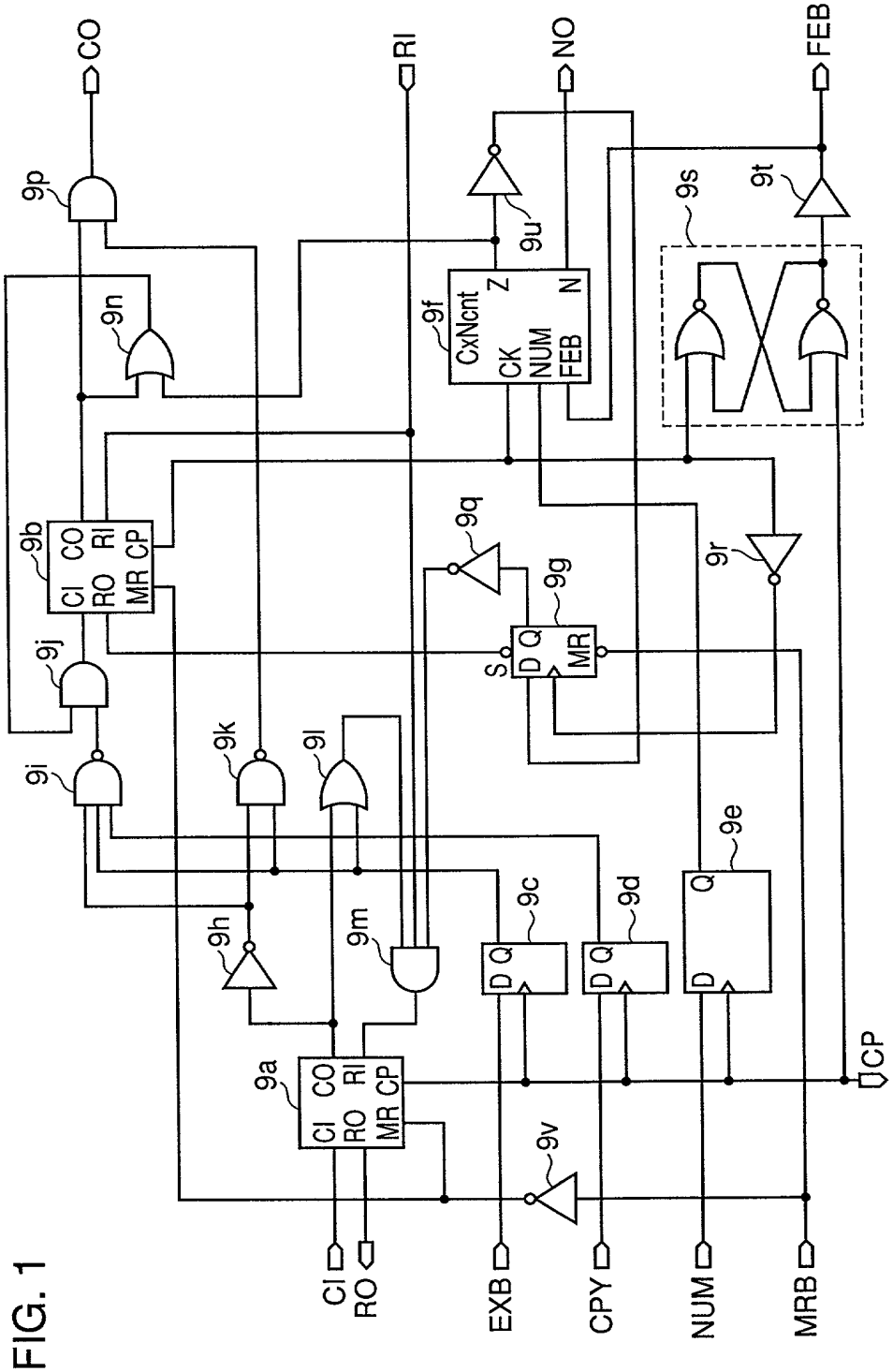
FIG. 1


CO
RI
NO
FEB
9p
9n
9f
CxNcnt
Z
N
CK
NUM
FEB
9u
9s
9t
9b
CI CO
RO RI
MR CP
9j
9i
9k
9l
9q
9g
9r
S
D Q
MR
9h
9m
9c
9d
9e
Q
D
9a
CI CO
RO RI
MR CP
9v
CP
CI
RO
EXB
CPY
NUM
MRB

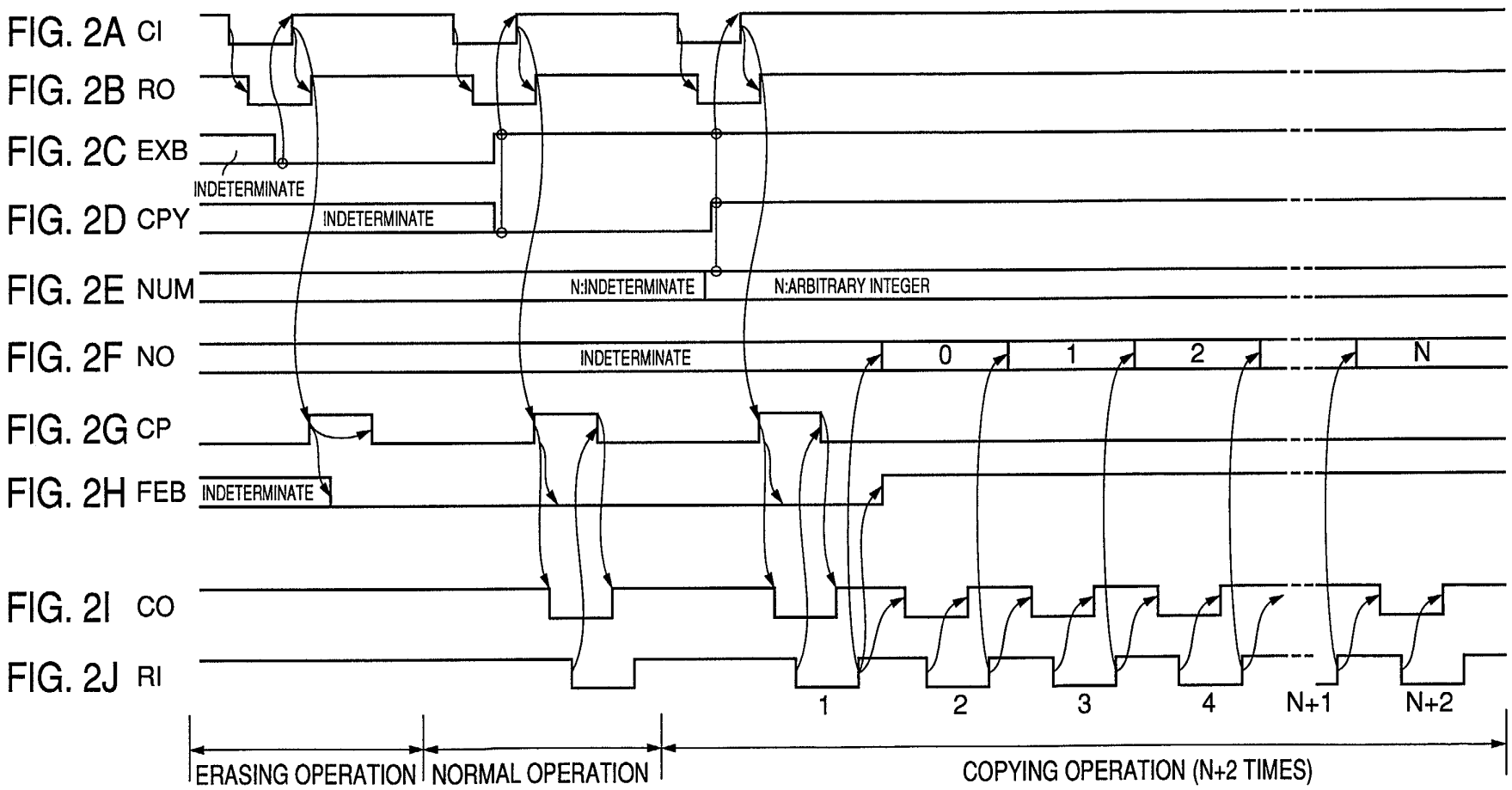


FIG. 3

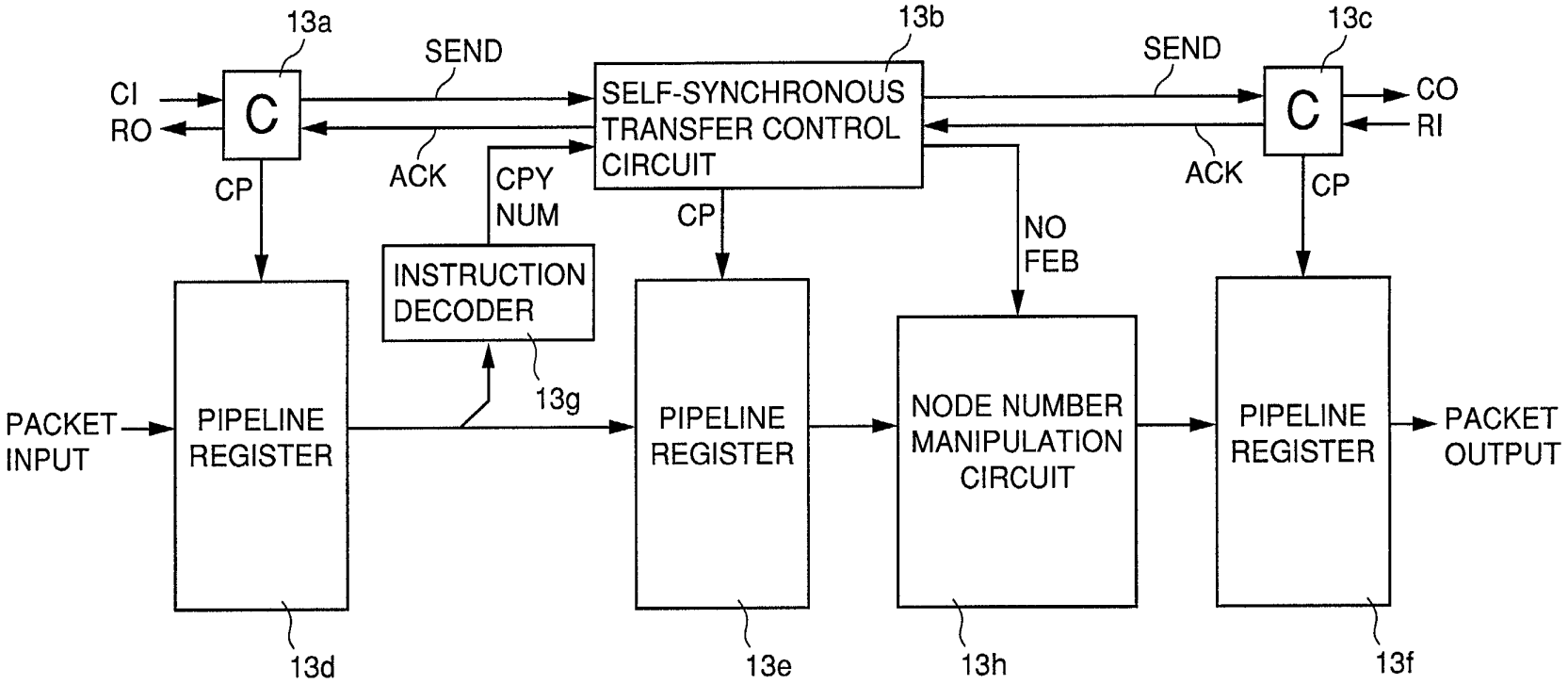

13a
13b
13c
SEND
SEND
CI
RO
C
SELF-SYNCHRONOUS
TRANSFER CONTROL
CIRCUIT
C
CO
RI
ACK
ACK
CP
CPY
NUM
CP
CP
NO
FEB
INSTRUCTION
DECODER
13g
PACKET
INPUT
PIPELINE
REGISTER
PIPELINE
REGISTER
NODE NUMBER
MANIPULATION
CIRCUIT
PIPELINE
REGISTER
PACKET
OUTPUT
13d
13e
13h
13f

FIG. 4A

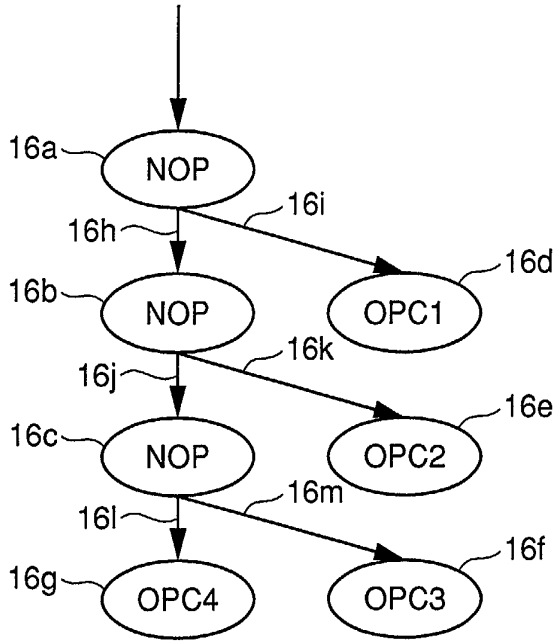

16a
NOP
16i
16h
16d
16b
NOP
OPC1
16k
16j
16e
16c
NOP
OPC2
16m
16l
16f
16g
OPC4
OPC3

FIG. 4B

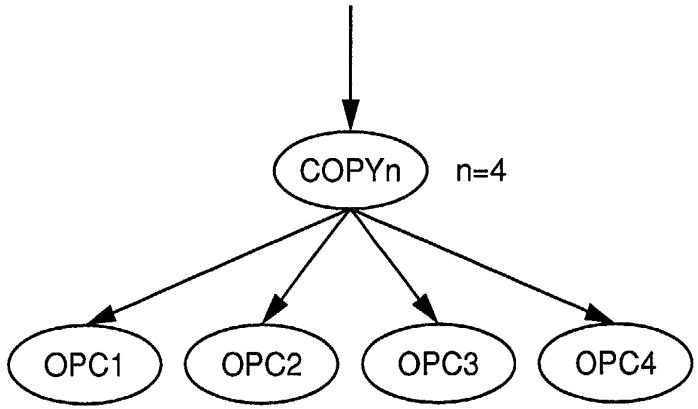

COPYn
n=4
OPC1
OPC2
OPC3
OPC4

FIG. 5

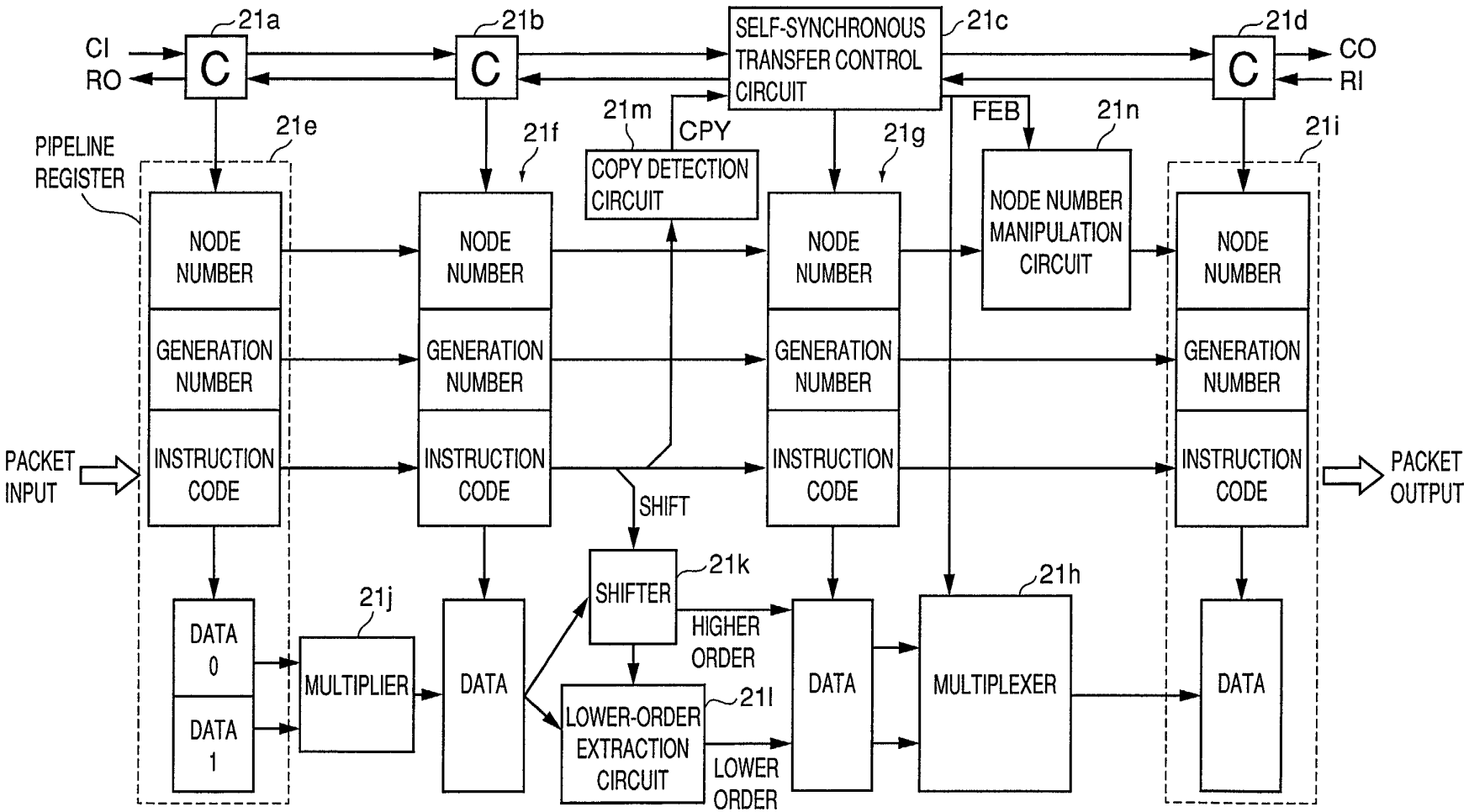
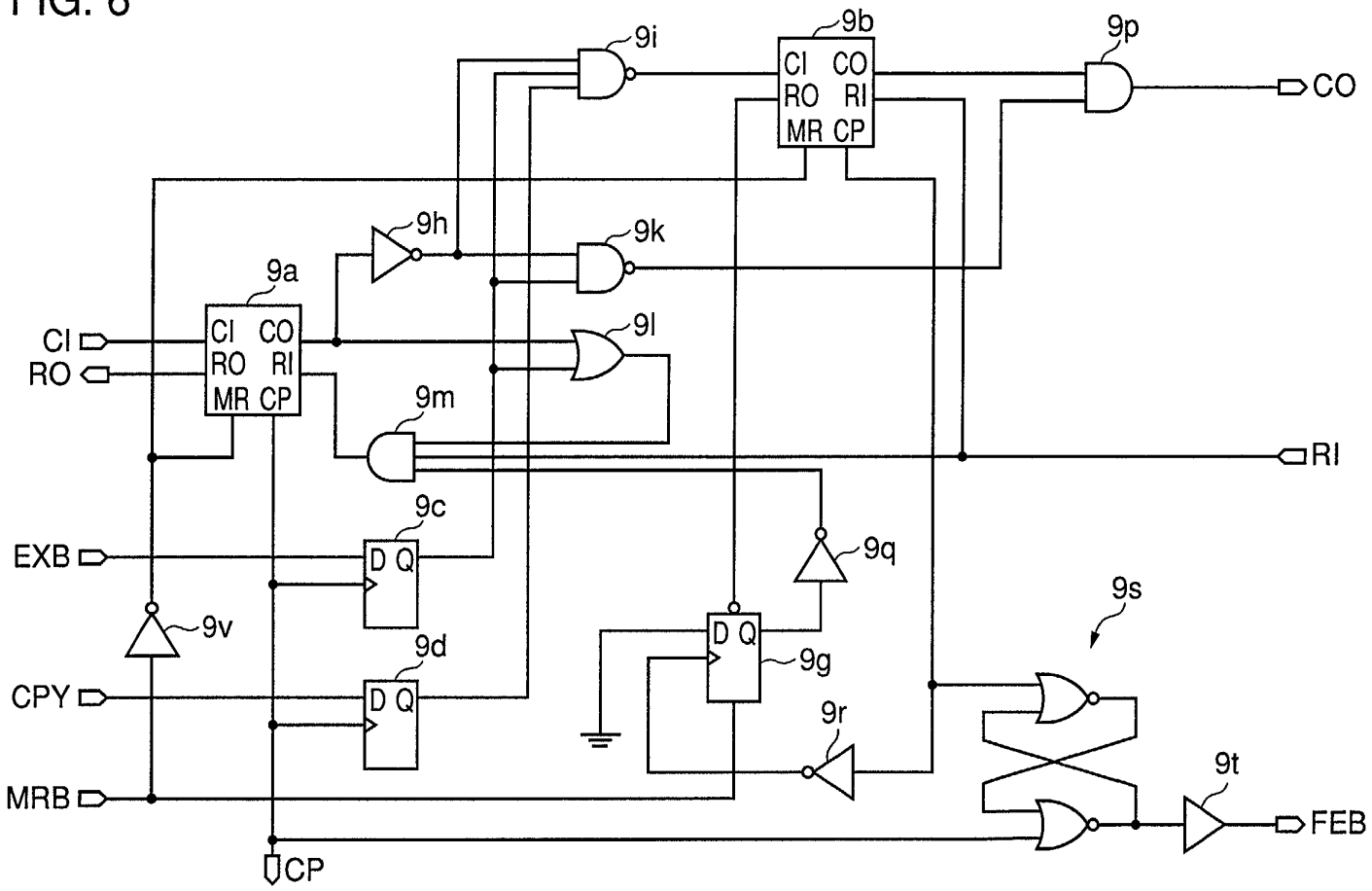

21a
21b
21c
21d
CI
RO
C
C
SELF-SYNCHRONOUS TRANSFER CONTROL CIRCUIT
C
CO
RI
21m
CPY
FEB
21n
21e
21f
21g
21i
PIPELINE REGISTER
COPY DETECTION CIRCUIT
NODE NUMBER MANIPULATION CIRCUIT
NODE NUMBER
GENERATION NUMBER
INSTRUCTION CODE
PACKET INPUT
PACKET OUTPUT
SHIFT
21k
SHIFTER
HIGHER ORDER
21h
21j
DATA 0
DATA 1
MULTIPLIER
DATA
LOWER-ORDER EXTRACTION CIRCUIT
21l
LOWER ORDER
MULTIPLEXER

FIG. 6


9i
9b
9p
CO
CI CO
RO RI
MR CP
9h
9k
9a
CI
RO
9l
9m
RI
9c
EXB
D Q
9q
9s
9v
9d
D Q
9g
CPY
9r
9t
MRB
FEB
CP

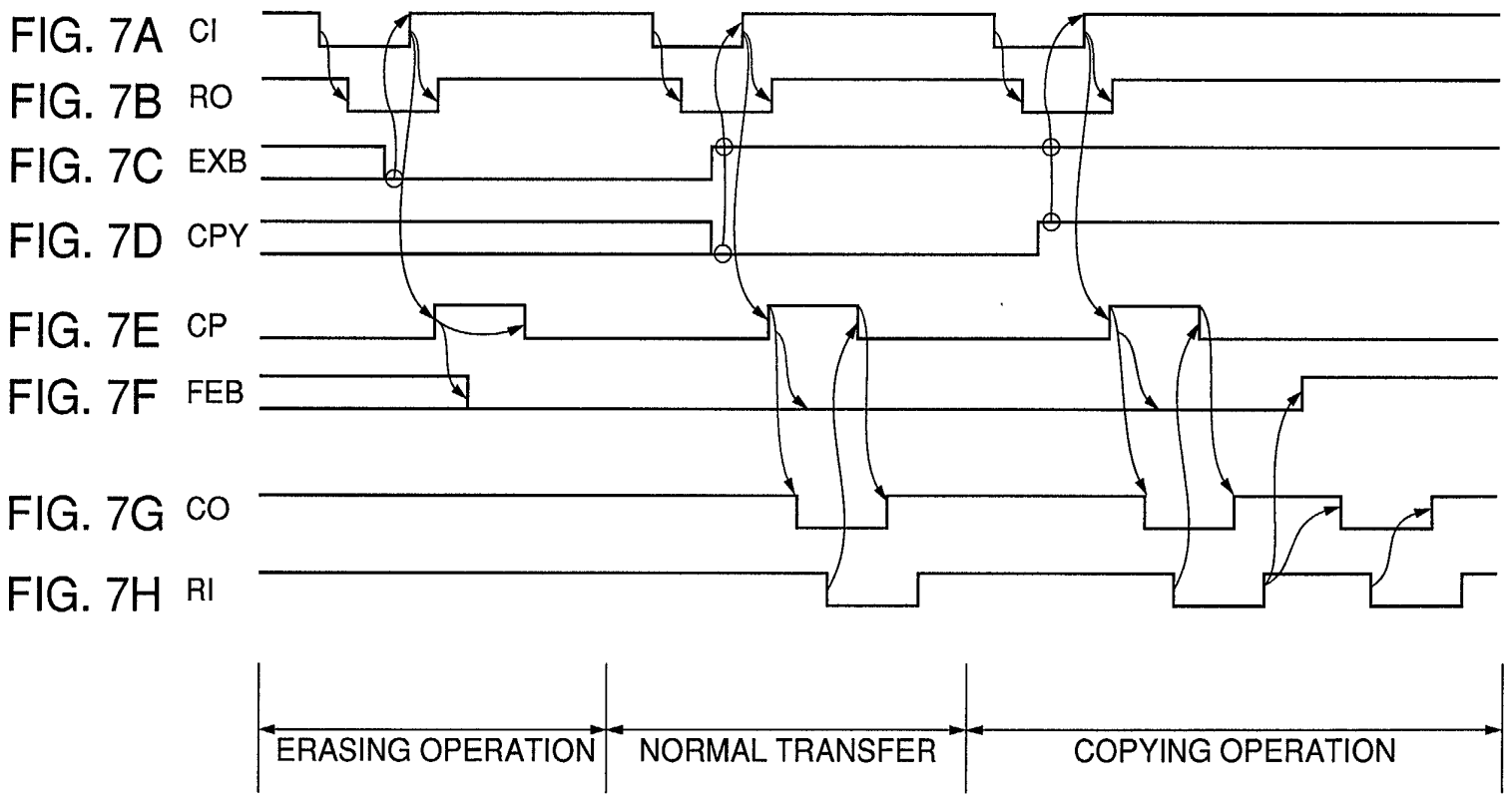


FIG. 8A

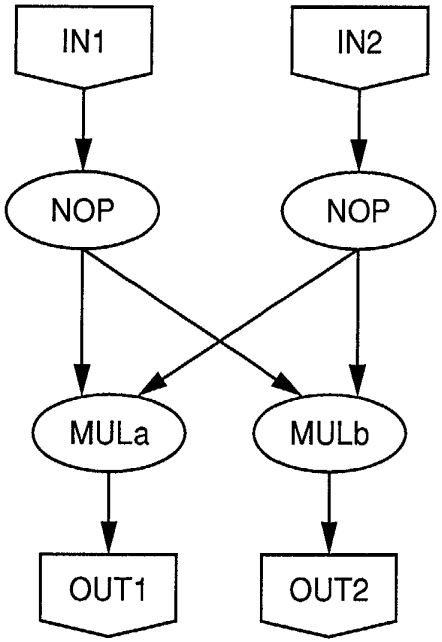


FIG. 8B

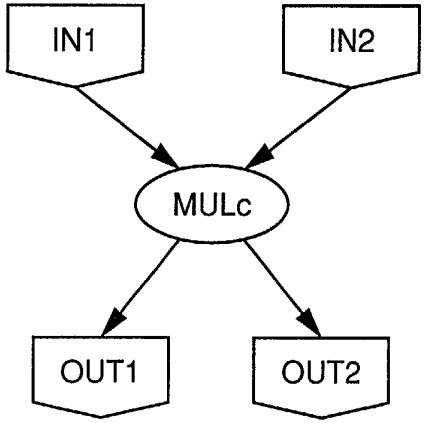


FIG. 9

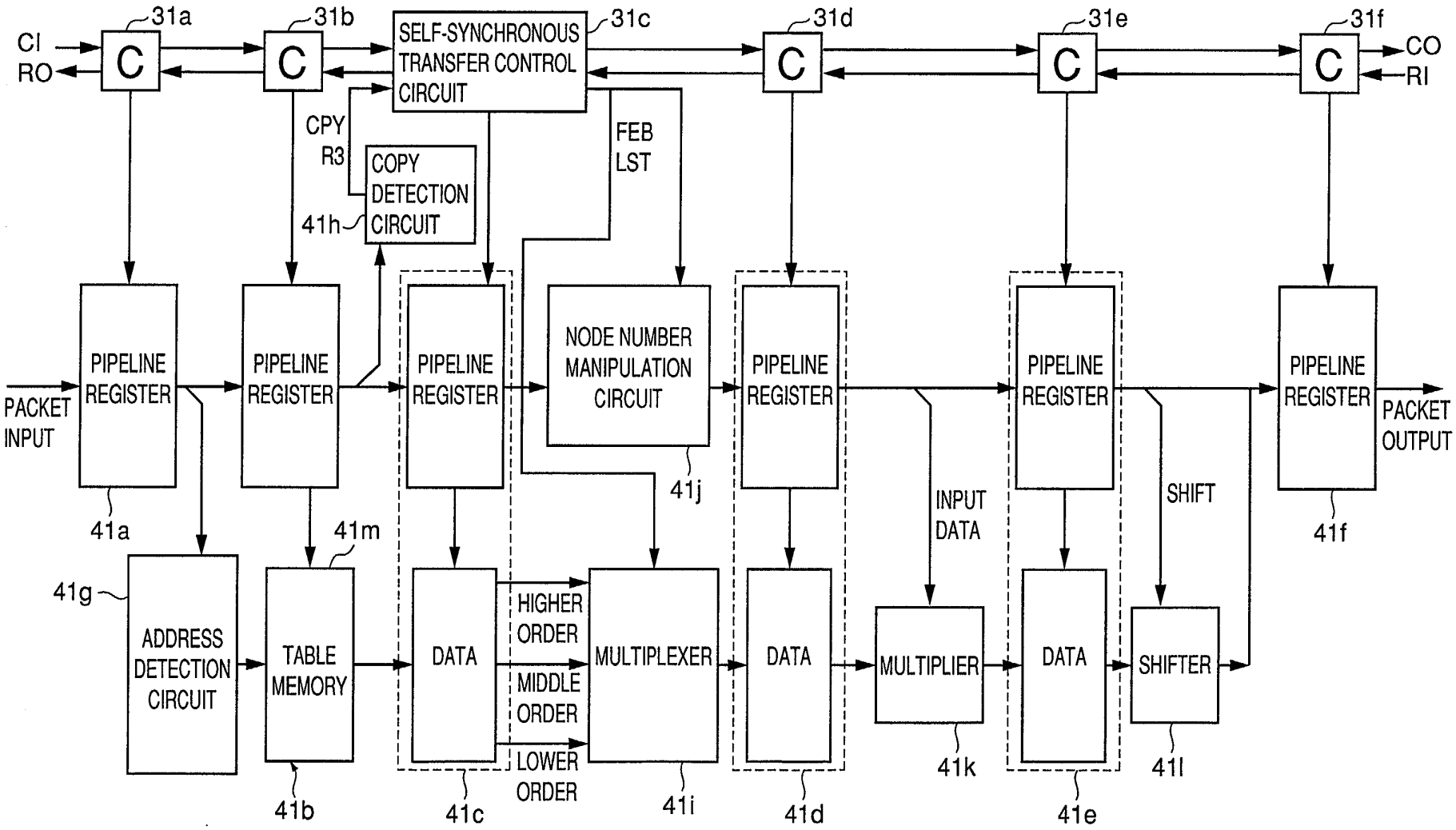

CI
RO
31a
C
31b
C
SELF-SYNCHRONOUS TRANSFER CONTROL CIRCUIT
31c
31d
C
31e
C
31f
C
CO
RI
CPY
R3
COPY DETECTION CIRCUIT
41h
FEB
LST
PACKET INPUT
PIPELINE REGISTER
PIPELINE REGISTER
PIPELINE REGISTER
NODE NUMBER MANIPULATION CIRCUIT
41j
PIPELINE REGISTER
PIPELINE REGISTER
PIPELINE REGISTER
PACKET OUTPUT
41a
41m
41f
INPUT DATA
SHIFT
41g
ADDRESS DETECTION CIRCUIT
TABLE MEMORY
DATA
HIGHER ORDER
MIDDLE ORDER
LOWER ORDER
MULTIPLEXER
DATA
MULTIPLIER
DATA
SHIFTER
41b
41c
41i
41d
41k
41e
41l

FIG. 10

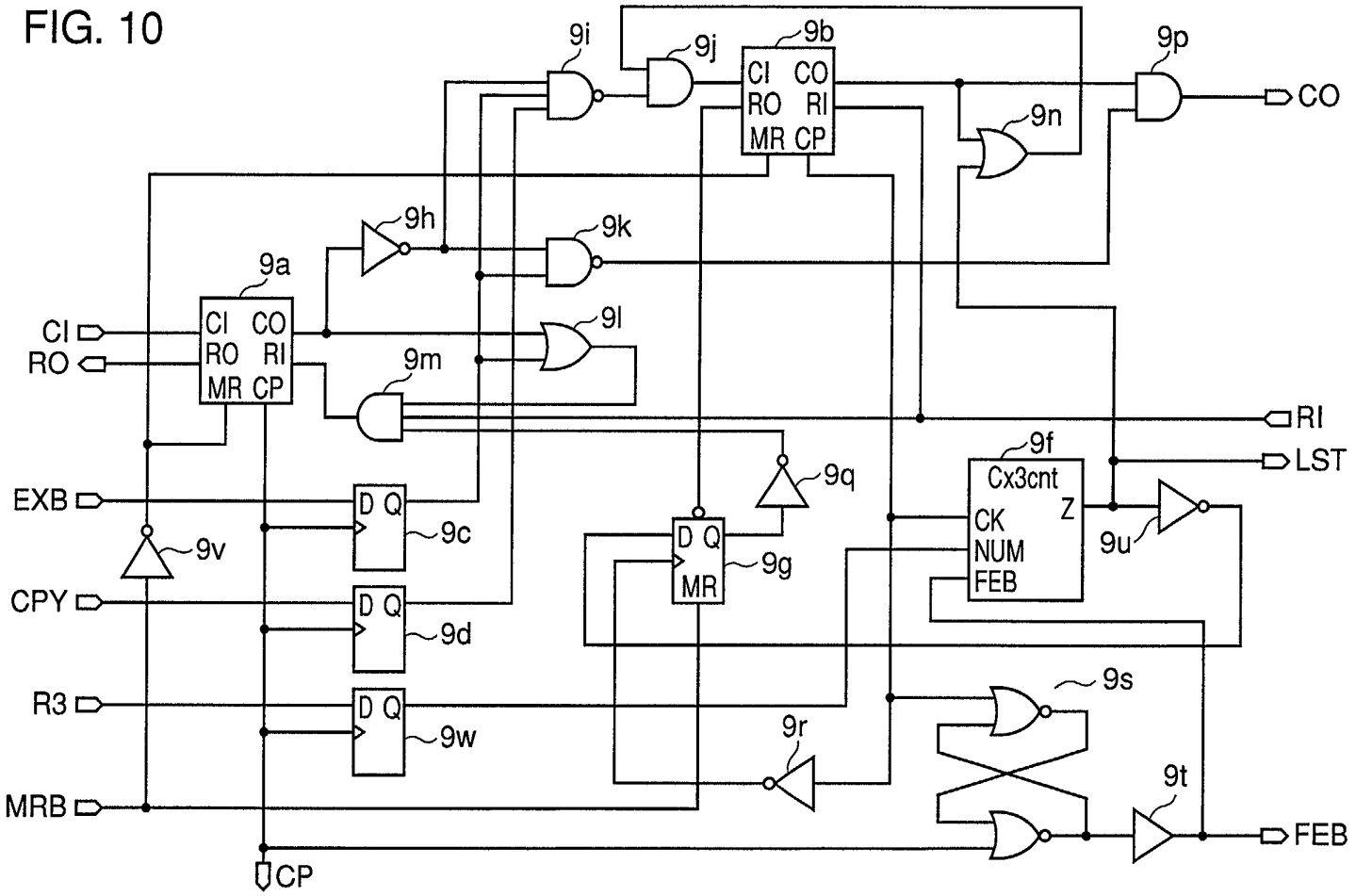

9i
9j
9b
CI CO
RO RI
MR CP
9p
CO
9n
9h
9k
9a
CI CO
RO RI
MR CP
CI
RO
9l
9m
RI
9f
LST
Cx3cnt
CK Z
NUM
FEB
9u
EXB
9q
D Q
9c
9v
D Q
MR
9g
CPY
D Q
9d
R3
D Q
9w
9s
9r
9t
MRB
FEB
CP

FIG. 11A
FIG. 11B
FIG. 11C
FIG. 11D
FIG. 11E
FIG. 11F
FIG. 11G
FIG. 11H
FIG. 11I
FIG. 11J

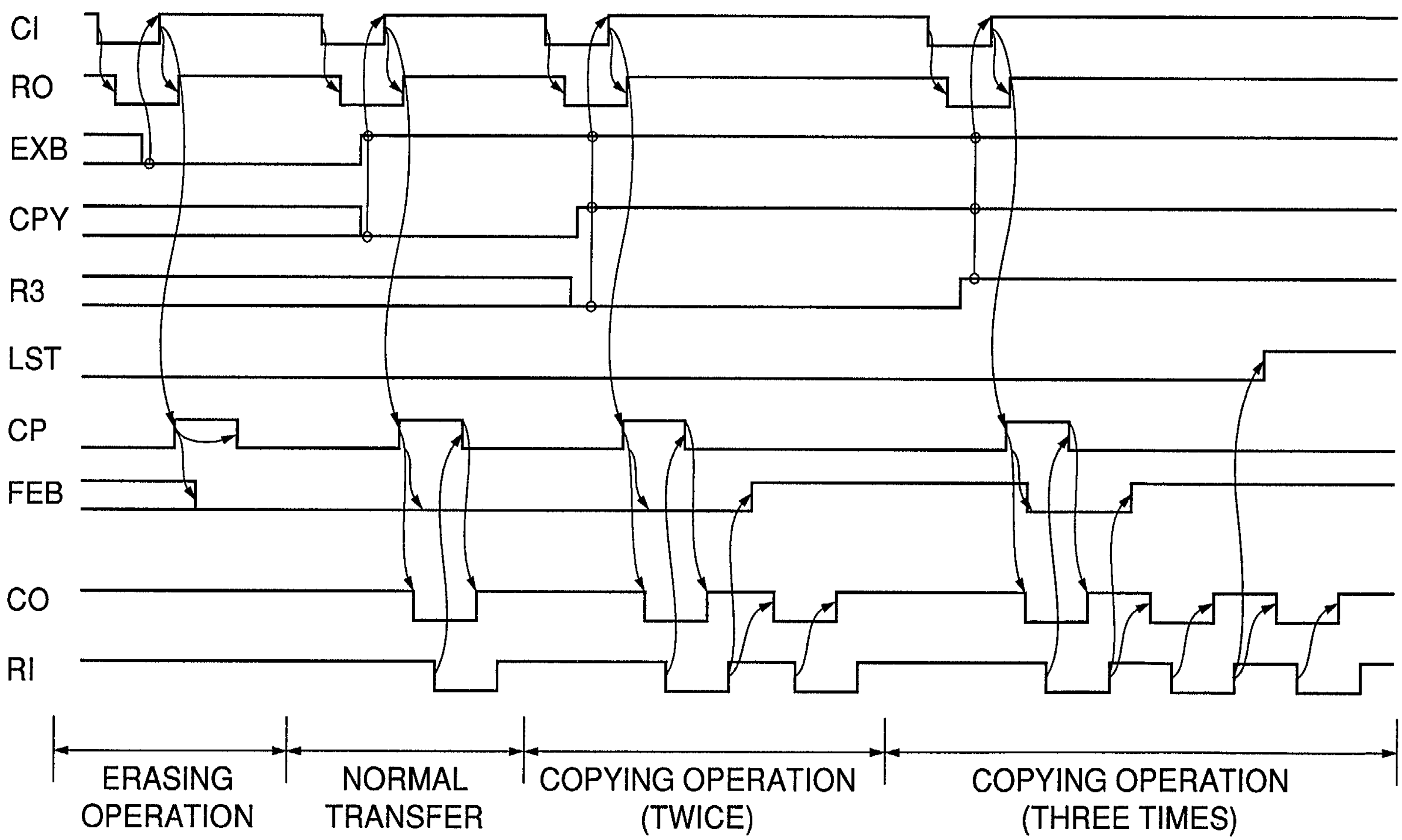
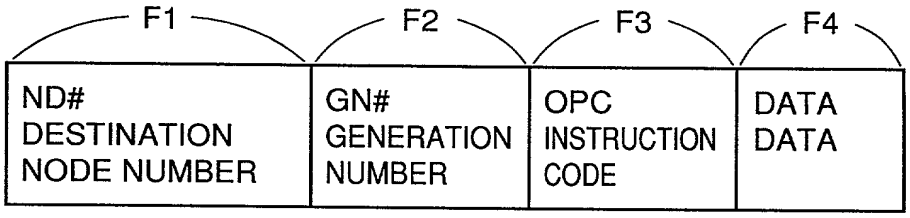


FIG. 12 PRIOR ART



F1: DESTINATION NODE NUMBER AREA
F2: GENERATION NUMBER AREA
F3: INSTRUCTION CODE AREA
F4: DATA REGION

FIG. 13 PRIOR ART

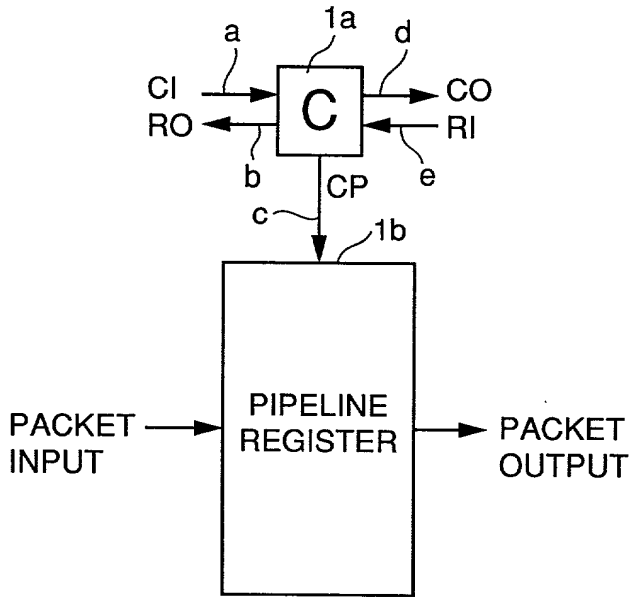


FIG. 14A PRIOR ART CI

FIG. 14B PRIOR ART RO

FIG. 14C PRIOR ART CP

FIG. 14D PRIOR ART CO

FIG. 14E PRIOR ART RI

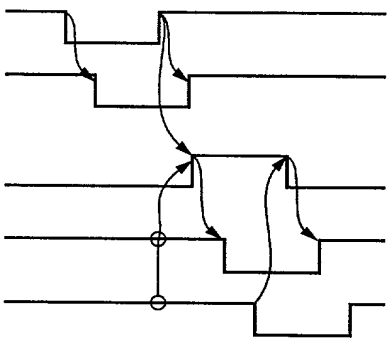


FIG. 15 PRIOR ART

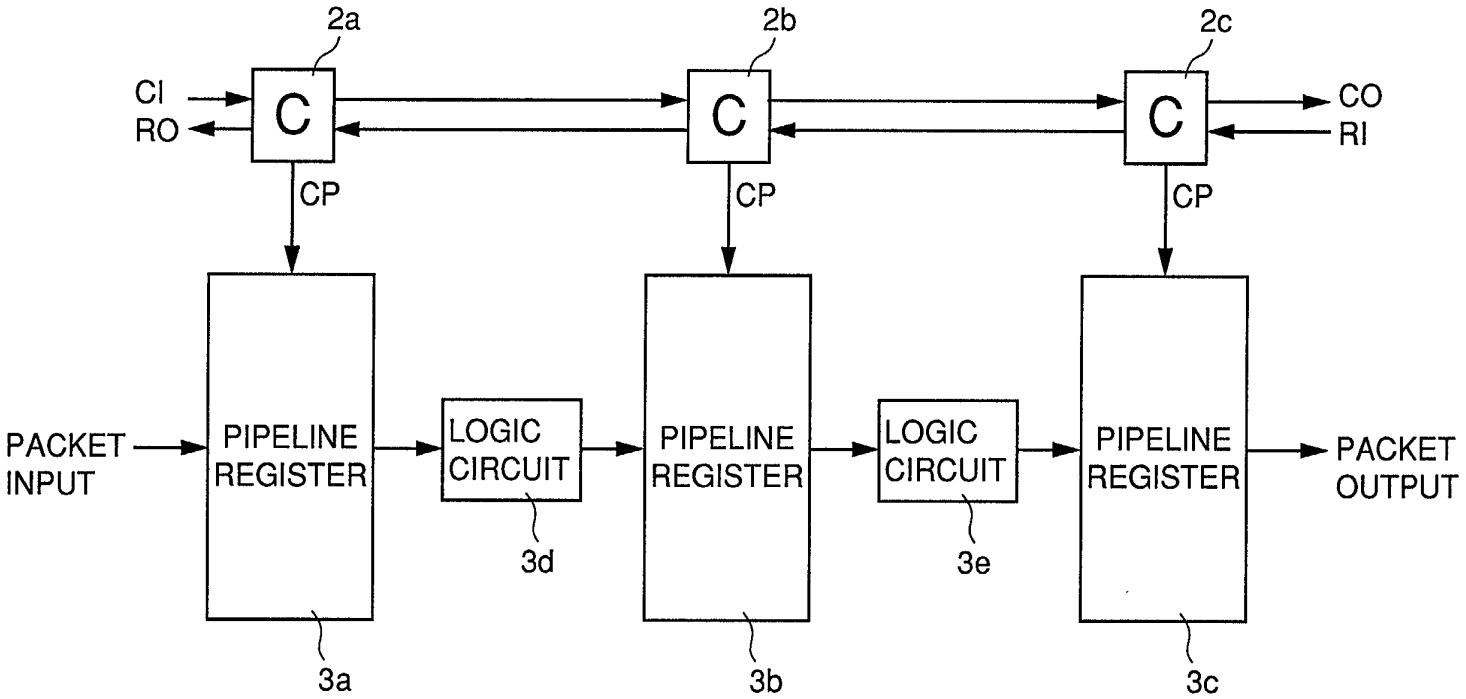


FIG. 16 PRIOR ART

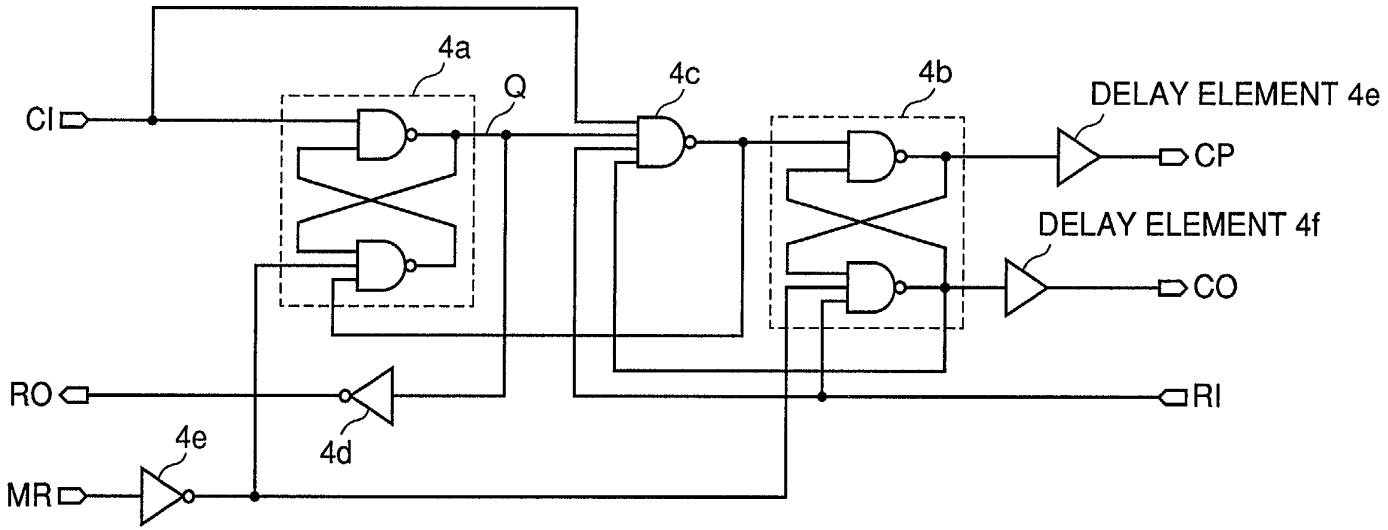


FIG. 17 PRIOR ART

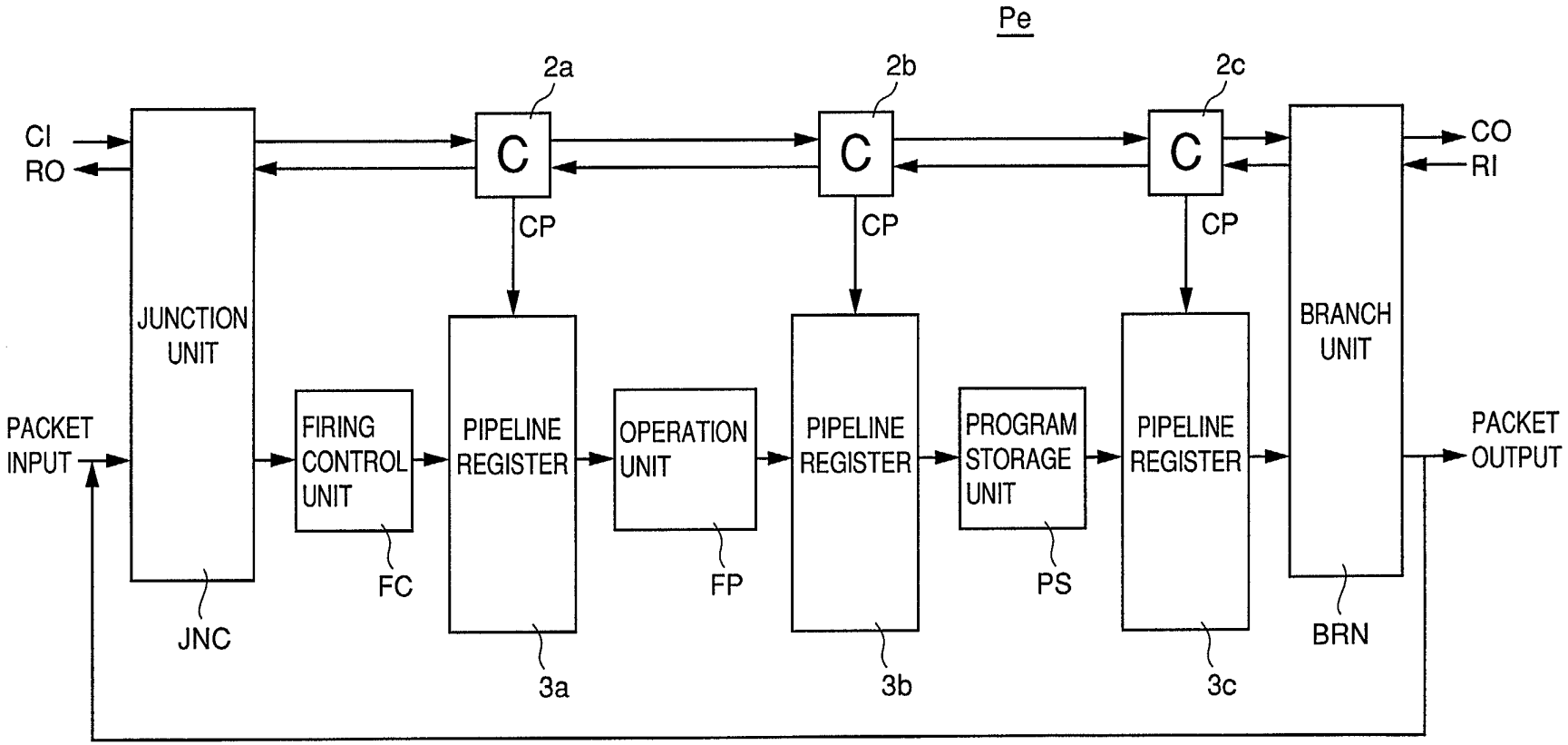


FIG. 18 PRIOR ART